IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): D.E. Parson et al.
Case: 3-2-1-4
Serial No.: 09/583,057
Filing Date: May 30, 2000
Group: 2114
Examiner: Timothy M. Bonura

Title: Control Method and Apparatus for Testing of Multiple Processor Integrated Circuits and Other Digital Systems

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Lisa M. Nanlis Date: September 10, 2004

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated May 10, 2004 in the above-referenced application, Applicants hereby request reinstatement of the appeal pursuant to 37 C.F.R. §1.193(b)(2). A Supplemental Appeal Brief is submitted concurrently herewith.

Respectfully submitted,

Joseph B. Ryan

Date: September 10, 2004

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Signature: Lewa M. Hamlin Date: September 10, 2004

Title: Control Method and Apparatus for Testing of Multiple Processor Integrated Circuits and Other Digital Systems

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SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is submitted in response to the Office Action dated May 10, 2004 in the above-referenced application, in which the Examiner reopened prosecution in response to the Appeal Brief filed February 17, 2004.

Applicants have submitted concurrently herewith a response to the Office Action, requesting reinstatement of the appeal.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

The present application was filed on May 30, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 13, 15, 19 and 20 are the independent claims.

Claims 1, 2, 4-6 and 8-20 stand rejected under 35 U.S.C. §103(a). Claims 3 and 7 are indicated as containing allowable subject matter. Claims 1, 2, 4-6 and 8-20 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the appealed rejection.

SUMMARY OF INVENTION

The present invention is directed to methods and apparatus for testing a digital system comprising a plurality of processors. In accordance with the invention, at least a subset of the processors are defined as forming a group of processors to be subject to common control, and issuance of one or more commands for the group of processors is delayed until a group scan command is received for each of the processors in the group.

An illustrative embodiment of the invention is in the form of a multiple processor test system 100 as shown in FIG. 1. The system 100 includes processors X, Y and Z, a debugger 102, a scheduler 104, and a chain manager 106, as well as Test Access Port (TAP) managers 108X, 108Y and 108Z for the respective processors X, Y and Z. The operation of the system 100 is described as follows at page 5, line 21 to page 6, line 9:

> The operation of the system 100 will now be described for a given test configuration involving a designated group of the multiple processors. The debugger 102 via the scheduler 104 asks the chain manager 106 for a group identifier (GROUP ID) for a group of known size. A particular member of a group refers generally to one of the processors and its corresponding TAP manager. The chain manager 106 issues a GROUP ID and stores that GROUP ID as well as the size of the group. This GROUP ID is passed back to the debugger 102. Each of the TAP managers 108X, 108Y and 108Z includes a device-specific program for its corresponding processor, and issues one or more IEEE 1149.1 scan commands ending

with a group scan command which may be, e.g., an instruction register (IR) command and/or a data register (DR) command.

A group scan command in the illustrative embodiment refers generally to a final JTAG scan command that occurs before a desired synchronous or pseudo-synchronous behavior. The group scan command generated by one of the TAP managers in a group is delayed by the chain manager 106 until the TAP managers for all other group members issue a group scan command. The individual commands of the groups are then merged, and synchronously and simultaneously scanned into the scan chain 110 by the chain manager 106.

The chain manager 106 thus delays the issuance of the group scan commands for the members of the group until all members of the group arrive at an equivalent state in their control sequences.

FIG. 4 shows a timing diagram illustrating the delayed issuance of one or more commands for a group of processors until a group scan command is received for each of the processors in the group. As described at page 10, line 27 to page 11, line 14, debugger 102 issues a command to each of a group of TAP managers denoted TAP 0, TAP 1 and TAP N, corresponding to respective processors 0, 1 and N, using a single non-zero GROUP ID. Each TAP manager translates its debugger command into a sequence of JTAG commands, but the JTAG chain manager 106 delays issuing the final group scan JTAG commands onto the JTAG hardware scan chain 110 until the arrival of the final JTAG command for TAP N, i.e., the group scan command for TAP N. The JTAG chain manager then issues the JTAG group scan commands for processors 0, 1 and N on the scan chain as a single synchronous bit stream. As a result, initiation or termination of processor execution, or of any other processor operation controlled by JTAG commands, is synchronized or pseudo-synchronized for processors 0, 1 and N. The JTAG chain manager 106 thus defers transmission of the JTAG command bit stream onto the JTAG hardware scan chain until the arrival of the final JTAG command for a group of processors with a shared GROUP ID.

The present invention in the above-described illustrative embodiments provides a number of significant advantages over conventional approaches. For example, the claimed arrangements

allow multiple processors to perform synchronous or pseudo-synchronous operations without requiring excessive coupling between individual processor debug systems as in conventional approaches. In addition, the processor grouping can be altered dynamically to allow for multiple groups of processors on the same scan chain and the alterations of these groups during a single debugging session. This control mechanism of the present invention is thus reusable for different numbers and arrangements of processors. See the specification at, for example, page 4, lines 9-16 and page 11, lines 16-21.

ISSUES PRESENTED FOR REVIEW

1. Whether claims 1, 2, 4-6, 8, 10, 12, 13, 15-17, 19 and 20 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 6,385,749 (hereinafter "Adusumilli") in view of U.S. Patent No. 6,173,386 (hereinafter "Key").

2. Whether claims 9 and 11 are unpatentable under §103(a) over Adusumilli and Key in view of the IEEE 1149.1 specification.

3. Whether claims 14 and 18 are unpatentable under §103(a) over Adusumilli and Key in view of U.S. Patent No. 4,135,240 (hereinafter "Ritchie").

GROUPING OF CLAIMS

With regard to Issue 1, claims 1, 4, 5, 8, 10, 12, 13, 19 and 20 stand or fall together, claim 2 stands or falls alone, claim 6 stands or falls alone, and claims 15-17 stand or fall together.

With regard to Issue 2, claims 9 and 11 stand or fall together.

With regard to Issue 3, claims 14 and 18 stand or fall together.

ARGUMENT

Issue 1

A proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill

in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in the §103(a) rejection of claims 1, 2, 4-6, 8, 10, 12, 13, 15-17, 19 and 20, in that the Adusumilli and Key references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

Each of independent claims 1, 13, 19 and 20 involves testing a digital system comprising a plurality of processors, and includes limitations relating to defining at least a subset of the processors as forming a group of processors to be subject to common control and delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

As noted above, the present invention as set forth in these claims provides a number of significant advantages over conventional approaches. For example, the claimed arrangements allow the multiple processors to perform synchronous or pseudo-synchronous operations without requiring excessive coupling between individual processor debug systems as in the conventional approaches. In addition, the processor grouping can be altered dynamically to allow for multiple groups of processors on the same scan chain and the alterations of these groups during a single debugging session. This control mechanism of the present invention is thus reusable for different numbers and arrangements of processors.

Applicants submit that the proposed combination of Adusumilli and Key fails to teach or suggest at least the above-noted limitations of each of independent claims 1, 13, 19 and 20, and furthermore fails to provide the associated advantages of the claimed invention.

The Examiner in formulating the §103(a) rejection acknowledges that Adusumilli fails to teach or suggest an arrangement in which the issuance of one or more commands for a group of processors subject to common control is inhibited or otherwise delayed until a group scan command is received for each of the processors in the group. See the May 10, 2004 Office Action at page 2,

section 3(b). However, the Examiner argues that such an arrangement would be obvious in view of Adusumilli and the teachings in Key at column 16, lines 11-21, 25-29 and 55-57. Applicants respectfully disagree. The relied-upon teachings from Key provide as follows:

> The external connection pin of line 291 may also supply the global fault signal to other components (e.g., BQU 210) of the switch system 200, as needed, to provide those components with indication that the processor 300 is entering global debug mode.
>
> When the MM 425 of an element 400 receives the global fault signal via line 291, the MM 425 transmits to the CPU 410 of that element 400 appropriate signals to indicate that it is desired for the element 400 to transition into debug mode from the element's normal mode of operation. In response to receiving these signals from the MM, the CPU provides appropriate signals to the coprocessor 475 to indicate that the element 400 is transitioning into debug mode. The MM 425, CPU 410 and coprocessor 475 then enter debug mode by halting their processing activities (while maintaining their respective internal states), and entering a "single step" processing mode. Thus, processing of each PE 400 is halted.
>
> . . .
>
> Thus, the element's processing is halted, but its internal state is maintained. The element's internal/data information may then be interrogated via interface 293 for facilitating debug operations.

Applicants submit that these teachings from Key, taken in conjunction with Adusumilli, fail to teach or suggest the claim limitation that calls for delaying the issuance of one or more commands for a group of processors subject to common control until a group scan command is received for each of the processors in the group. The Key teachings relied upon by the Examiner instead relate to a global fault signal, which as indicated in column 15, line 64, to column 16, line 4, is generated "upon supply of an appropriate debug trigger signal . . . from an external source . . . , or supply of a global exception signal generated by on-chip fault monitoring logic . . . ." The global fault signal of Key does not teach or suggest delaying issuance of commands for a group of processors until certain commands are received for each of the processors of the group. Instead, it automatically halts all of

the processors, as indicated in the above-quoted passages. This not only fails to meet the limitation in question, but actively teaches away from it.

Applicants respectfully submit that the collective teachings of Adusumilli and Key fail to provide any teaching or suggestion of forming a group of processors to be subject to common control and delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group. As mentioned previously herein, one possible example of such a group scan command in an illustrative embodiment of the present invention is described as follows at page 6, lines 1-9, of the specification:

> A group scan command in the illustrative embodiment refers generally to a final JTAG scan command that occurs before a desired synchronous or pseudo-synchronous behavior. The group scan command generated by one of the TAP managers in a group is delayed by the chain manager 106 until the TAP managers for all other group members issue a group scan command. The individual commands of the groups are then merged, and synchronously and simultaneously scanned into the scan chain 110 by the chain manager 106.
>
> The chain manager 106 thus delays the issuance of the group scan commands for the members of the group until all members of the group arrive at an equivalent state in their control sequences.

Such an arrangement is simply not met by the collective teachings of Adusumilli and Key.

Each of claims 1, 13, 19 and 20 thus includes one or more limitations which are not taught or suggested by the proposed combination of Adusumilli and Key. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection.

Also, as indicated previously, the Examiner has failed to identify a cogent motivation for combining the references or for modifying the reference teachings to reach the claimed invention.

As was described above, neither Adusumilli nor Key teaches or suggests the limitation of claims 1, 13, 19 and 20 that calls for delaying the issuance of one or more commands for a group of

processors subject to common control until a group scan command is received for each of the processors in the group. However, the Examiner argues that it would be obvious to combine or modify the teachings of these references to meet the limitation in question.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. There has been no showing in the present §103(a) rejection of objective evidence of record that would motivate one skilled in the art to combine Adusumilli and Key or to modify the proposed combination of Adusumilli and Key to produce the claim limitations.

The statement of obviousness provided by the Examiner at page 3, first paragraph, of the May 10, 2004 Office Action is a conclusory statement of obviousness, that mischaracterizes the reference teachings and fails to address the particular limitations at issue. For example, the statement argues that Adusumilli in lines 43-44 of column 2 discloses "a need to wait for the test signals." This is believed to be a misreading of the passage in question, which provides as follows:

> Another aspect of the present invention is directed to a method for controlling multiple test-access port (TAP) controllers coupled to a common interface for a multi-core IC having a limited number of access pins for selecting functions internal to the IC. The method comprises: at each of the multiple TAP controllers, receiving input signals, determining if the TAP controller is enabled, and generating status and test signals; in response to each of the multiple TAP controllers, outputting one of the test signals respectively provided by the multiple TAP controllers; and at the input of each of the multiple TAP controllers, providing the input signals and for maintaining one of the TAP controllers enabled at a given time.

The Examiner argues that the above passage "discloses that the TAP controllers generates [sic] status and test signal in response to these signals." To the extent that this argument is understandable, Applicants believe that it mischaracterizes the content of the passage, in that there is nothing in the passage that suggests a "a need to wait for the test signals" as alleged. In any case, the relied-upon passage fails to provide the requisite motivation for combination of Adusumilli with Key or modification of their teachings to reach the limitations of the independent claims.

It appears, in view of the conclusory statement of obviousness provided by the Examiner, that the Examiner in combining Adusumilli and Key has simply undertaken a hindsight-based piecemeal reconstruction of the claimed invention based on the disclosure provided by Applicants. Such an approach is improper.

Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner. For example, the above-quoted passage from column 2, lines 43-44 of Adusumilli indicates that only "one of the TAP controllers [is] enabled at a given time." It is believed that this is a direct teaching away from the claimed invention, which calls for delaying the issuance of one or more commands for a group of processors subject to common control until a group scan command is received for each of the processors in the group. Such a teaching away constitutes evidence of non-obviousness.

Applicants therefore respectfully submit that independent claims 1, 13, 19 and 20 are allowable over Adusumilli and Key.

Dependent claims 4, 5, 8, 10, 12 are believed allowable for at least the reasons identified above with regard to their respective independent claims.

With regard to dependent claim 2, this claim calls for defining a group of processors in a chain manager in response to a group request received from a debugger. The Examiner argues that this limitation is obvious in view of Adusumilli and Key, relying particularly on column 16, lines 21-25, of Key. However, the collective teachings of the cited references fail to meet the particular language of the limitation in question. This teaching from Key, in combination with the teachings from Adusumilli, fails to teach or suggest the claimed defining of a group of processors in a chain manager in response to a group request received from a debugger.

With regard to dependent claim 6, this claim specifies that each processor and its corresponding TAP manager may have membership in only one group at a given point in time. The Examiner argues that this limitation is obvious in view of Adusumilli and Key, relying on column 2, lines 12-16, of Adusumilli. The relied-upon passage fails to provide any teaching regarding the particular limitation of claim 6. Thus, the collective teachings of the cited references fail to meet the particular language of the limitation in question.

With regard to independent claim 15, this claim calls for a chain manager coupled to a command generator, where the chain manager is operative to define at least a subset of a plurality of processors as forming a group of processors to be subject to common control, to receive one or more of the test commands for each of the processors in the group, and to delay issuance of at least a subset of the test commands for the group until a designated group scan command is received for each of the processors in the group. The Examiner relies again on Adusumilli and Key, but the collective teachings of these references fail to disclose or suggest a chain manager of the type set forth in the claim. Also, for the reasons presented above, no objective evidence of motivation for combination or modification of Adusumilli and Key has been identified.

Dependent claims 16 and 17, which depend from independent claim 15, are believed allowable for at least the reasons identified above with regard to claim 15.

Issue 2

Dependent claims 9 and 11, which depend from independent claim 1, are believed allowable for at least the reasons identified above with regard to claim 1.

The arguments presented above with regard to independent claim 1 are realleged and incorporated herein by reference. The IEEE 1149.1 specification fails to supplement the fundamental deficiency of the proposed combination of Adusumilli and Key as applied to claim 1.

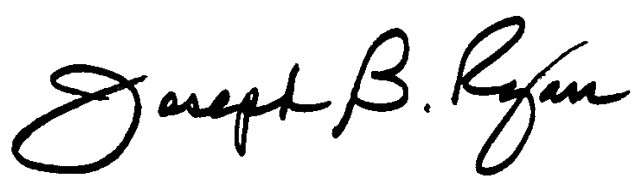
Issue 3

Dependent claims 14 and 18, which depend from independent claims 13 and 15, respectively, are believed allowable for at least the reasons identified above with regard to claims 13 and 15.

The arguments presented above with regard to independent claims 13 and 15 are realleged and incorporated herein by reference. The Ritchie reference fails to supplement the fundamental deficiency of the proposed combination of Adusumilli and Key as applied to claims 13 and 15.

In view of the above, Applicants believe that claims 1, 2, 4-6 and 8-20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,



Date: September 10, 2004

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APPENDIX

1. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control; and

delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

2. The method of claim 1 wherein the defining step includes defining the group of processors in a chain manager in response to a group request received from a debugger.

3. The method of claim 2 wherein the chain manager establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger.

4. The method of claim 1 wherein the commands comprise commands configured in accordance with the IEEE 1149.1 standard.

5. The method of claim 1 wherein the group scan commands for each of the processors in the group are generated by a Test Access Port (TAP) manager associated with the corresponding processor.

6. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of only one group at a given point in time.

7. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of different groups of processors at different points in time.

8. The method of claim 1 wherein the group of processors comprises a group of homogeneous processors.

9. The method of claim 8 wherein the delaying step provides synchronous control for the group of homogeneous processors.

10. The method of claim 1 wherein the group of processors comprises a group of heterogeneous processors.

11. The method of claim 10 wherein the delaying step provides pseudo-synchronous control for the group of heterogeneous processors.

12. The method of claim 1 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied as a single serial bit stream to a hardware scan chain associated with the processors.

13. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, and to delay issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

14. The apparatus of claim 13 wherein the chain manager is implemented at least in part in software.

15. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a debugger;

a scheduler coupled to the debugger and operative to generate in response to signals from the debugger a set of debug commands for the processors;

at least one test command generator coupled to the scheduler and operative to generate test commands from the debug commands;

a chain manager coupled to the command generator and operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more of the test commands for each of the processors in the group, and to delay issuance of at least a subset of the test commands for the group until a designated group scan command is received for each of the processors in the group.

16. The apparatus of claim 15 further comprising a plurality of test command generators, with one of the test command generators associated with each of the processors.

17. The apparatus of claim 15 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied by the chain manager as a single serial bit stream to a hardware scan chain associated with the processors.

18. The apparatus of claim 15 wherein the chain manager is implemented at least in part in software.

19. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control;

receiving one or more commands for each of the processors in the group; and

delaying issuance of at least a subset of the commands for the group until a group scan command is received for each of the processors in the group.

20. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more commands for each of

the processors in the group, and to delay issuance of the commands for the group until a designated group scan command is received for each of the processors in the group.